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INTEGRATED OPTICAL 2x2 SWITCH FOR WAVELENGTH MULTIPLEXED INTERCONNECTS

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Abstract - A highly compact integrated optical switch is proposed and demonstrated for broadband optical switching applications. A scheme is proposed to leverage the advantages of lossless operation, broad optical bandwidth and nanosecond switching times. Wavelength multiplexing is exploited for reduced latency, enhanced capacity and functionality, while retaining compatibility with existing off-the-shelf electronics and transceiver technology. The requirement for optical header processing, wavelength translation and optical buffering is avoided. Low-penalty multi-wavelength transmission is demonstrated for a highly compact sub-mm² amplifying 2x2 switch. Pattern dependent gain and amplified spontaneous emission are minimized to facilitate 0.0-0.4dB penalty. Mitigation techniques compatible with architecture are deployed to reduce the penalty for operating regimes where signal distortion occurs. Control schemes are proposed and demonstrated to facilitate 8x10Gb/s optically switched networking.

Index terms - Integrated optoelectronics, optical switches, optical interconnection, wavelength division multiplexing, semiconductor optical amplifiers, packet switching

I. INTRODUCTION

Switch fabrics with nanosecond reconfiguration times are of particular interest in optical interconnects and access networks [1 **Sengupta**], but such applications are highly cost sensitive, and performance metrics such as capacity, efficiency and latency are key. Considerable research has addressed the role of optical switch fabrics in the metropolitan area network, tackling the demanding problems of high line rate all optical processing, optical synchronization and optical read/write of routing information [2 **Toliver**, 3 **Emery**]. The optical complexity of the complete switch fabric and the requirement for custom transceiver technologies have therefore made such approaches unsuited to low-cost high-capacity applications. It is therefore of interest to investigate how highly compact integrated switch fabrics may be implemented with available data networking technologies.

A wide range of optical switch fabrics have been proposed to facilitate nanosecond timescale path reconfiguration [4 **Renaud**]. Switches exploiting phase modulation include directional couplers [5 **Hamamoto**] and Mach Zehnder modulators [6 **Duthie**] have been fabricated in 8x8 matrices and higher. Wavelength agile systems have avoided matrix implementations by using NxN passive wavelength routers [7 **Bregni**]. Loss modulators have been implemented as arrays in conjunction with wavelength routers [8 **Ido**]. Semiconductor optical amplifiers (SOA) have been demonstrated as both gate arrays [9 **Sahri**] and matrix switches with dimension up to 4x4 [10 **van Berlo**]. The relative advantages of the published fabrics are well understood in terms of the optical performance. To identify optimum technologies for a specific application also requires a comparison of implementation. Table 1 compares a number of switch technologies, which have been investigated and tested in packet routing environments.

Comparing available fabrics purely in terms of the optical performance reveals that the inherent regenerative properties of electronic switch fabrics used in conjunction with a

series of point to point links is highly attractive for moderate transmission rates. Wavelength tuned switching facilitates routing by means of electronic control through a passive wavelength router and therefore does not suffer significant optical impairments either. The remaining active optical switching technologies outlined in table 1 do all however incur additional optical power penalties, whether it is crosstalk, noise, loss or signal impairment. While polarisation dependence has been a common problem, careful design has allowed this to be minimized [8 Ido, 10 van Berlo, 11 Nishimoto].

When comparing the implementation of switching technologies for the case of the switched optical interconnect, the electronic solutions reveal significant disadvantages. The additional transceivers required for each wavelength in an electronic fabric are an undesirable power drain and together with the required de/multiplexers at the switch occupy a large board area. For wavelength routing, the required control schemes can impair latency. Multi-hop networking would rely on immature wavelength translation technologies. A wavelength imposed granularity will determine the minimum packet length and in turn latency. Active switching schemes, however, offer the potential for broadband routing. No de/multiplexers are required at the fabric, enabling much more compact solutions. Wavelength multiplexed packets may be compressed in time relative to single channel packets to enable higher packet throughput and therefore offer the potential for reduced latency.

While in the telecomms environment ideal optical performance has been key to tolerate a wide range of transmission imperfections, optical specifications in the data storage and data networking environments are more relaxed. Due to the net gain available, SOA switch fabrics have been investigated for single wavelength transmission in discrete [12 Shibata] monolithic [10 van Berlo, 13 Burton, 14 Djordjevick] and hybrid [15 Kato] implementations. Investigations on the wavelength multiplexed performance have however been limited to cascaded SOA repeaters for long distance transmission [16 Crijs] and to gain-clamped SOA gain blocks amplifying switched data [17 Spiekman]. In this work, we propose a highly compact integrated optical add drop multiplexer and characterize the performance for four wavelength transmission. Low penalty operation is observed when operated in the non-saturated regime to indicate that cascaded switch

nodes are feasible. When operated with increased current and therefore higher gain, a low penalty is still maintained for wavelength multiplexed payloads.

In this work, we explore the potential of amplifier switching technologies in the switched interconnect environment as this technology offers highly compact, lossless, low drive current solutions based on established technologies for a cost sensitive environment. The broadband routing functionality avoids channel granularity and allows for reduced optical complexity, and reduced optical component count relative to electrical switch fabrics. Section II proposes a scheme such that design trade offs may be identified, and SOAs used. Section III proposes a highly compact switch fabric, which is well suited to the proposed architecture. Section IV characterizes the performance under wavelength multiplexed operation and switched operation.

II. WAVELENGTH MULTIPLEXED SWITCHED INTERCONNECT

To fully leverage the advantages of SOA based switched fabrics and ensure compatibility with increasingly high performance electronic circuits and transceiver technologies, an architecture has been devised for high capacity packet routing. Figure 1 shows a three node interconnect implementation based on 2x2 switches. The photonic component count has been reduced at the switch to just moderate speed data transceivers for the control channel. Low cost data transceiver technologies are implemented at a higher data rate. The media access control and therefore contention resolution is handled at the network edge where electronic buffers are available as a matter of course. In tandem with the short link lengths envisaged, this avoids the requirement for optical memory. A separate control channel is implemented to configure the switches. This avoids deep packet inspection which would either impose a bottleneck on the transmission speed or lead to the requirement for delays and high performance electronics at the switch.

The switch is operated without a need to appreciate the content of the data packets. Off the shelf transceiver technologies are therefore used to ensure a low cost solution.

Indeed, low cost GBIC technologies are used for the control channel. A distinguishing feature for data protocols has been the use of high transition count coding schemes such as 8B10B to facilitate low complexity clock and data recovery [18 Cunningham]. Such schemes may therefore be further exploited to mitigate patterning in the switch fabric. It is for this reason that the switch fabrics in this work are characterized for short pattern lengths as well as the more conventional long test patterns associated with telecom specifications.

In this work we implement the switch within a test-bed with WDM transmitters centered at 1550nm interfacing to wavelength and data rate agnostic switches. The switch is configured using an out of band 1310nm uncooled transceiver which interfaces to the control logic directly. Passive low loss, 1310/1550nm multiplexers as developed for passive optical networks (PON) are implemented for combining the control and data signals. A considerable component count reduction is achieved as data transceivers and data channel demultiplexers are dispensed with at the switch. As the multi-wavelength packets are compressed in time, and as no inline processing is performed at the optical switch, latency can be significantly reduced.

The sub-network is time slotted for the routing of fixed length packets. The use of idle tones when not transmitting data avoids transients in the switch, and facilitates the use of AC coupled transceivers. While the path losses will be comparable, leading to a low dynamic range requirement at the receiver, the sub-network is semi-synchronous in that the bit level clock will change for consecutive packets [19 Mac]. In this work, the non-optimum clock recovery used and guard band restraints allow for 0.5 μ s packet transmission with 85% time slot utilization.

III. INTEGRATED OPTICAL ADD DROP MULTIPLEXER

A. Mode of operation

The optical switch fabric is based on a split and gate concept [13 Burton], using four highly compact waveguide splitters and four semiconductor amplifier gates. This integrated component allows the same functionality as a two input two output crosspoint switch and a wavelength agnostic add drop multiplexer. Figure 2 shows a schematic layout which highlights the four splitters, four gates and the input and output waveguides. The gate electrodes form the output paths for each of the four splitters. The optical paths are configured electrically by biasing the amplifier gates for either loss or gain to switch the optical signals. The electrical control scheme is summarized in table 2.

The gates are labeled A through to D and form the output guides of four waveguide splitters. The splitters also form the input and output waveguides. Input 1 and output 1 are on opposing facets, but input 2 and output 2 have been routed to a third facet for ease of assessment in this work. It is worth highlighting that designs with all the waveguides on the two opposing facets have been fabricated by rotating input 2 and output 2 by $+90^\circ$ degrees and -90° respectively. This allows for ease of facet coating as bars and also reduced complexity in subsequent packaging.

The mode of operation for the integrated switch structures is identical. As no regrowth is used, all the input and output guides must be biased. A current of 10mA per splitter is sufficient to ensure gain. The four gates labeled A, B, C and D which form the central square are configured to define the optical path through the switch. In the off state, the loss of the gate blocks the signal. In the on state, a current of between 10-40mA may be applied to overcome splitter and coupling losses. As shown in table 2, the device may be operated as a broadband time slot multiplexer or as a 2x2 crosspoint switch. It may also

be configured for broadcast operation. More complex wavelength interleaving functions may be envisaged with appropriate transmitter control.

B. Fabrication

The add drop multiplexer is fabricated using a single stage quantum well epitaxial growth with ridge waveguide processing [20 CST fab runs]. The active layer is designed for C-band operation. Patterned p-type electrodes facilitate individual addressing of the amplifier gates and inputs. The isolation between the electrodes exceeds 700Ω for all electrode combinations. An image of the 2x2 switch fabric is shown in figure 3. The input and output guides each include a linearly tapered mode expander, which terminates at one of four mode splitters. The splitters comprise 45° totally internal reflecting mirror to route light into the perpendicular guide as well as a through path. The mirrors are fabricated by focused ion beam etching [21 Roberts]. The waveguide spacing is $250\mu\text{m}$ and the input and output guides are $350\mu\text{m}$ leading to a highly compact overall chip area of $850 \times 850\mu\text{m}^2$. The input and output ports are anti-reflection coated to 0.3%, and the add and drop ports exiting via the third facet and are as cleaved in the tested device.

C. DC characteristics

Continuous wave measurements have been performed between input, output, add and drop ports and indicate a splitting ratio of 45:55. The discrepancy is readily accommodated through fine tuning of the SOA currents. On chip gain, inclusive of splitter losses is measured to be 7dB and 15dB for operating currents of 20mA and 30mA per SOA respectively. The add and drop paths denoted by input 2 and output 2 in figure 2 include a cleaved facet with 0.3 reflection, and so this can lead to a noticeable gain

ripple at high operating currents. The operating current for the add and drop ports is reduced to facilitate tolerable wavelength dependent gain.

IV. DYNAMIC OPERATION

A. Port to port characterization

The WDM test-scheme comprises a four wavelength source centered at 1550nm with 200GHz spacing modulated 2.488 Gb/s data. Data is decorrelated by means of fibre delays. The modulated data is aggregated with an arrayed waveguide grating prior to launch into the switch ports. The device is temperature stabilised and operated with an aggregate input power of -6dBm. A schematic diagram for the assessment arrangement is shown in figure 5.

Initial measurements are performed for 20mA per gate, corresponding to a chip power requirement of less than 20mW per SOA. Power penalty was assessed for 10^{-10} bit error rate by monitoring the received channels in sequence. No error floors are observed for the operating currents of 20mA per gate as shown for the bit error rate plots shown in figure 4. Power penalty performance is summarized by wavelength and path in table 2. For the input to output path, where the facets are anti-reflection coated, penalties from 0.0-0.4dB are measured. This degrades on both add and drop paths and is attributable to the 2dB gain ripple on the cleaved add and drop outputs.

The distortion and noise degradation due to the optical switch fabric is readily quantified in terms of the power penalty incurred. A linear interpolation is made to the bit error rate data in figure 5, and the difference between the back to back and switched data paths is

derived for each wavelength channel. As values are subject to experimental measurement accuracy, values are quoted to one decimal place.

The power penalties are measured to be lowest for the antireflection coated through path, with wavelength dependent values varying from 0.0dB to 0.4dB. The add and drop channels both have one cleaved facet, and are therefore susceptible to enhanced gain ripple. This degrades the signal to noise performance for channels 2 and 4 for drop and add paths respectively due to reduced gain for a fixed level of amplified spontaneous emission.

B. Wavelength and pattern dependence of power penalty

Low penalty is readily demonstrated for optimum operating conditions, which are representative of operating conditions in the proposed architecture. It is also of interest to explore the limits to the switch performance for high gain as this may facilitate additional splitters and therefore higher port count fabrics. Operation at the elevated bias currents and therefore higher SOA gain does lead to an excess power penalty. This penalty degradation has been investigated by varying the pseudo random bit sequence length and also the number of wavelength channels. Figure 5 shows the power penalty for gates operated at 26mA for a range of pseudo random bit sequence lengths and wavelength channel numbers. A significant pattern dependent penalty is observed for low wavelength channel numbers. At higher wavelength numbers however, the penalty and is less dependent on the pseudo random bit sequence for the test data used and also reveals power penalty reduction under wavelength multiplexed operation. Further increases in bias current lead to further degradation in penalty. At 30mA per gate, a wavelength dependent penalty of 0.3-3.3dB per gate is observed for four wavelength transmission.

For an increased operating current the gain increases and the input saturation power is lowered. The resultant distortion results from a carrier lifetime which is of the order of one nanosecond will be comparable to the bit period. This is therefore sensitive to the

pseudo random bit sequence used. It is noted that in a data-communications environment, high transition count coding schemes are implemented routinely to relax transceiver design and such implementations would be advantageous to reducing power penalty in SOA based switching.

The wavelength dependence of the power penalty is attributable to residual facet reflections and is therefore readily improved through the use of lower reflectivity coatings. Mitigation due to multiple wavelength transmission is anticipated to result from the higher number of transitions apparent at the amplifiers. By maintaining a low power penalty without compromising either gain or input power, the wavelength channel number and therefore aggregate throughput may be optimized.

C. Switched operation

The gate electrodes are switched according to the required paths and the states are given in table 2. To demonstrate packet routing operation, the switch is configured in the test-bed shown in figure 8. The test-bed emulates one of the nodes in figure 1 and the first 2x2 switch to which the node connects. The switch is configured using an out of band wavelength channel which is sent to the Xilinx Virtex II Pro field programmable gate array (FPGA) which configures the switch. This in turn outputs the signals to the drivers to configure the gates as required [22 Lin].

The packet payload comprises eight wavelengths which are data modulated with a customized data sequence at 10Gb/s. The repeated sequence includes a packet preceded by a 64 byte dark guard band and includes a 30 byte clock assist preamble of alternating ones and zeros and a 546 byte payload comprising the first part of a $2^{13}-1$ pseudo random bit sequence. The guard-band is limited by the 2-3 cycle jitter for the FPGA, corresponding to up to 48ns for the 62.5MHz clock used. The pattern generator requires that data blocks are multiples of 32 bytes, and the length of the payload is defined by the

clock recovery attribute of the error detector. The resulting packet slot time is therefore $0.512\mu\text{s}$ and the ratio of payload duration to time slot is 0.85.

The control channel bit rate to the switch operates at 1250Mb/s to facilitate full addressing and switch control for multiple destinations. The GBIC transceiver interfaces to the high speed Rocket I/O ports. The control information precedes the packet payload to allow processing time. A switch driver waveform is generated to configure the optical switch to route the desired multi-wavelength packet. At the data transmitter, eight distributed feedback lasers centered 1550nm are multiplexed and amplified.

The switch is used to drop one of four repeated packets and is assessed in terms of error performance. Figure 9 shows the waveforms for the input and output signals from the switch. Stable, error free operation is demonstrated, as shown in the bit error rate diagram in figure 9.

The data channel payload has been defined to operate with the error analyzer, and therefore the restrictions on the efficiency are anticipated to be relaxed as increased intelligence is used in the transmitter.

V. DISCUSSION

An architecture is proposed which allows the deployment of optical switching using largely available technologies. A highly compact, power efficient optical switch solution is proposed. A 2x2 fabric is used to facilitate routing of data rates of 8x10Gb/s without the additional optical signal processing used in telecommunications based demonstrators.

The power penalty incurred by the switch is low on the AR coated path, from 0.0dB to 0.4dB depending on the channel selection. This is readily improved by using a range of low facet reflectivity designs including mode field optimization, angled facets and multilayer coatings. This may also be improved by reduced the input power, although the input optical power of -6dBm selected is consistent with the envisaged architecture. The

add and drop functionality is confirmed for multi-wavelength operation. The losses associated with the integrated splitter are negligible. Further improvements in loss and power consumptions might be anticipated through the use of butt coupled active passive integration, or through intermixing technologies. A switch further suited to packaging is proposed and fabricated whereby the inputs and outputs are aligned on opposing facets. The 250 μ m pitch is suited to fiber ribbon technology.

While gain ripple and distortion is avoided by operating a switch in the low gain regime suitable for 2x2 switches, high gain operation has also been explored. This mode of operation may be of interest for larger port count switch fabrics where increased splitter loss may be anticipated. The trade off between crosstalk and gain places contradictory design requirements, and so it is of interest to explore routes to distortion mitigation. It is shown that uncorrelated multi-wavelength coding, where high transition counts are ensured, allows for improved operation, and this mode of operation is particularly well suited to the short switched data links envisaged.

VI. CONCLUSIONS

A fully integrated SOA based add-drop multiplexer is demonstrated for WDM networking applications. The switch facilitates low power switching of wavelength compressed packets with lossless operation and low distortion penalty even when operated with high input power. The switch has been demonstrated in packet routing applications.

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References

- [1] S. Sengupta, V. Kumar and D. Saha, "Switched optical backbone for cost-effective scalable core IP networks", *IEEE Communications Magazine*, 60-70, June 2003
- [2] P. Toliver, I. Glesk, R.J. Runser, K.L. Runser, K.L. Deng, B.Y. Yu and P.R. Prucnal, "Routing of 100Gb/s words in a packet-switched optical networking demonstration (POND) node", *IEEE Journal of Lightwave Technology*, 16, 2169-2180, 1998.
- [3] J.Y. Emery, E. Grard and M. Renaud, "Physical and logical validation of a network based on all-optical packet switching systems", *IEEE Journal of Lightwave Technology*, 16, 2255-2264, 1998
- [4] M. Renaud, M. Bachmann and M. Erman, "Semiconductor optical space switches", *IEEE Journal of Selected Topics in Quantum Electronics*, 2, 277-288, 1996
- [5] K. Hamamoto, T. Anan, K. Komatsu, M. Sugimoto and I. Mito, "First 8x8 semiconductor optical matrix switches using GaAs/AlGaAs electro-optic guided-wave directional couplers", *Electronics Letters*, 28, 441-443, 1992
- [6] P.J. Duthie and M.J. Wale, "16x16 single chip optical switch array in Lithium Niobate", *Electronics Letters*, 27, 1265-1266, 1991
- [7] S. Bregni, A. Pattavina and G. Vegetti, "Architectures and performance of AWG-based optical switching nodes for IP networks", *IEEE Journal of Selected Areas in Communications*, 21, 1113-1121, 2003
- [8] T. Ido, M. Koizumi, S. Tanaka, M. Suzuki and H. Inoue, "Polarisation and wavelength insensitive MQW electroabsorption optical gates for WDM switching systems", *IEEE Photonics Technology Letters*, 8, 788-790, 1996

- [9] N. Sahri, D. Prieto, S. Silvestre, D. Keller, F. Pommerau, M. Renaud, O. Rofidal, A. Dupas, F. Dorgeuille and D. Chiaroni, "A highly integrated 32-SOA gates optoelectronic module suitable for IP multi-Terabit optical packet routers", OFC 2001
- [10] W. van Berlo, M. Janson, L. Lundgren, A.C. Morner, J. Terlecki, M. Gustavsson, P. Granstrand and P. Svensson, "Polarisation-insensitive, monolithic 4x4 InGaAsP-InP laser amplifier gate switch matrix", IEEE Photonics Technology Letters, 16, 102-104, 2004
- [11] H. Nishimoto, S. Suzuki and M. Kondo, "Polarisation independent LiNbO₃ 4x4 matrix switch", Electronics Letters, 24, 1122-1123, 1988
- [12] Y. Shibata, Y. Yamada, K. Habara, and N. Yoshimoto, "Semiconductor Laser Diode Optical Amplifiers/Gates in Photonic Packet Switching", IEEE Journal of Lightwave Technology, 16, (12), 2228-2235, 1998
- [13] J.D. Burton, P.J. Fiddymment, M.J. Robertson and P. Sully, "Monolithic InGaAsP-InP laser amplifier gate switch matrix", IEEE Journal of quantum electronics, 29, (6), 2023-2027, 1993
- [14] I.B. Djordjevic, R. Varazza, M. Hill and S.Yu, "Packet switching performance at 10Gb/s across a 4x4 optical crosspoint switch matrix", IEEE Photonics Technology Letters, 16, 102-104, 2004.
- [15] T. Kato, J. Sasaki, T. Shimoda, H. Hatakeyama, T. Tamanuki, S. Kitamura, M. Yamaguchi, T. Sasaki, K. Komatsu, M. Kitamura and M. Itoh, "Hybrid integrated 4x4 optical matrix switch module on silica based planar waveguide platform", IEICE Transactions on Communications, E82-B, 357-360, 1999.
- [16] J. Crijns, L.H. Spiekman, G.N. van den Hoven, E. Tangdionga, H. de Waardt, "Static and dynamic switching performance of a metro WDM ring using linear optical amplifiers", IEEE Photonics Technology Letters, 14: 1481-1483, 2002.

- [17] L.H. Spiekman, J.M. Wiesenfeld, A.H. Gnauck, L.D. Garrett, G.N. van den Hoven, T. van Dongen, M.J.H. Sander-Jochem, J.J.M. Binsma, "8 x 10 Gb/s DWDM transmission over 240 km of standard fiber using a cascade of semiconductor optical amplifiers", IEEE Photonics Technology Letters 12, 1082-1084, 2000
- [18] D. Cunningham and W.G. Lane, Gigabit Ethernet, MacMillian, 1999
- [19] D. McAuley, "Optical Local Area Network", in Computer Systems: Theory, Technology and Applications, A. Herbert and K. Sparck-Jones, Eds. Springer-Verlag, February 2003
- [20] Epitaxial growth provided by IQE Ltd, Cardiff UK, and ridge waveguide fabrication by CST Global Ltd, Glasgow, Scotland
- [21] G.F. Roberts, K.A. Williams, R.V. Penty, I.H. White, M. Glick, D. McAuley, D.J. Kang, M. Blamire, "Monolithic 2x2 amplifying add/drop switch for optical local area networking", ECOC 2003
- [22] T. Lin, W. Tang, K.A. Williams, G.F. Roberts, R.V. Penty, I.H. White, M. Glick and D. McAuley, "80Gb/s optical packet routing for data networking using FPGA based 100Mb/s control scheme", ECOC 2004

Figure captions:

Figure 1: Proposed collapsed ring architecture for 2x2 SOA based switches

Figure 2: Schematic diagram of 2x2 SOA fabric showing modes of operation

Figure 3: Image of the fabricated and bonded device, showing the detail of the waveguide splitter with totally internally reflecting (TIR) mirror

Figure 4: Spectral width of 32nm covers the C band

Figure 5: Test procedure for multi-wavelength transmission through switch

Figure 6: Bit error rate curves for the output, add and drop paths for wavelength channels: $\blacktriangle \lambda_1$, $\blacklozenge \lambda_2$, $\bullet \lambda_3$, $\blacksquare \lambda_4$, where open symbols indicate back to back measurement and filled symbols indicate the signal passes through the switch

Figure 7: Role of channel count and pattern on power penalty. Pseudo random bit sequences used: $\bullet 2^4-1$, $\blacksquare 2^7-1$ and $\blacktriangle 2^{15}-1$.

Figure 8: Schematic diagram of packet routing test-bed

Figure 9: Bit error map for switched data

Switch technology	Electronic core	Phase modulation	Wavelength tuning	Loss modulation	Gain modulation
Implementations	Point to point WDM fibre links	Mach-Zehnder Directional couplers	Fast tunables with wavelength routers	Channel blockers	SOA gates
Optical characteristics	✓✓ Regenerative	✗ Moderate loss ✗ Moderate crosstalk ✓ No added noise ✓ No added distortion	✓ Low loss ✓ Low crosstalk ✓ No added noise ✓ No added distortion	✗✗ High loss ✓ Low crosstalk ✓ Low noise ✓ Low distortion	✓ Lossless ✓ Low crosstalk ✗ 7dB noise figure ✗ Distortion prone
Channel granularity	✗ Narrowband ✓ Broadcast possible	✓ Broadband ✗ No broadcast	✗ Narrowband ✗ No broadcast	✗ Moderate bandwidth ✓ Broadcast possible	✓ Broadband ✓ Broadcast possible
Electrical characteristics	✗ Added transceivers	✗ High switch voltage	✗ Additional control	✓ Low switch voltage	✓ Low switch voltage
Footprint	✗ Added transceivers ✗ Added de/multiplexer	✗ Large footprint switch	✗ Large footprint router	✓ Compact	✓ Compact

Table 1: A comparison of key technologies for switching with nanosecond reconfiguration times in wavelength multiplexed fiber optic links

Path	Gate A	Gate B	Gate C	Gate D
Input 1 to output 1	High	-	Low	-
Input 1 to output 2	-	High	-	Low
Input 2 to output 1	Low	-	High	-
Input 2 to output 2	-	Low	-	High
<i>Crosspoint operation</i>				
Bar state (1 to 1; 2 to 2)	High	Low	Low	High
Cross state (1 to 2; 1 to 1)	Low	High	High	Low
<i>Broadcast operation</i>				
Input 1 (1 to 1 and 2)	High	High	Low	Low
Input 2 (2 to 1 and 2)	Low	Low	High	High

Table 2: Modes of operation for the integrated add drop multiplexer showing bias levels for gates A to D as defined in figure 2

Path	λ_1	λ_2	λ_3	λ_4	units
Through	0.1	0.4	0.0	0.3	dB
Add	0.6	0.3	0.5	1.1	dB
Drop	0.6	1.2	0.7	0.7	dB

Table 3: Error penalties at 10^{-10} for the through path, add and drop paths at 20mA per gate for a pseudo random bit sequence of 2^7-1 . Measurements are performed for four wavelength channels through the switch